REMARKS

I. Status of Claims

After the above amendments, claims 1-22 are pending. Claims 1, 9, 21 and 22 are independent. Claims 1 and 9 have been amended to better clarify the claims and claims 17-22 are new.

II. Rejections under 35 U.S.C. §102(e) as being anticipated by SHIN et al. (US 2004/0006734 A1)

The Examiner has maintained the rejections of claims 1-16 under 35 U.S.C. §102(e) as being anticipated by SHIN et al. (US 2004/0006734 A1), hereafter SHIN. Applicants respectfully request reconsideration of the rejections because SHIN neither explicitly nor implicitly, discloses, teaches, suggests, nor anticipates each and every limitation of the claims. In particular, starting with independent claim 1, the claim requires:

> A method for controlling a decoder when a first data and a second data are successively received in a mobile communication system, comprising the steps of:
>
> a) decoding the first data;
>
> b) determining the completion status of the decoder; and
>
> c) interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data **at a decoding start time of the second data**

(emphasis added).

Applicants respectfully disagree with the Examiner that SHIN anticipates claim 1. Specifically, Applicants argues that at the least SHIN fails to anticipate "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data" as recited in Applicants' claim 1.

SHIN's teaching is directed toward minimizing a delay for generating an ACK/NACK response signal in a User Equipment (UE). To do so, SHIN determines if iterations in an H-

ARQ process either converge, diverge or reach a maximum number of iterations. If the iterations in the H-ARQ process either converge or diverge, an ACK or NACK is respectively generated. Thereby, a delay for generating an ACK/NACK response signal is reduced.

By contrast, the subject matter of claim 1 includes controlling a decoder when a first data and a second data are successively received. Further, claim 1 includes "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data". By way of example, the above subject matter is beneficial in that it allows for plural bocks to be decoded by a single decoder in a single H-ARQ process. Further, by another example, the above subject matter is beneficial in that it allows for the entire response (ACK/NAK) time delay of the first data to be divided for the decoding of the first and second data. Therefore, SHIN differs from the subject matter in claim 1 in that in SHIN's teaching, the iterations of decoding for an H-ARQ process are minimized so as to generate the ACK/NACK response signal with minimal delay, whereas the subject matter of claim 1 allows for the decoding of plural data within the response (ACK/NAK) time delay of the first of plural data.

In the Examiner's comments listed on page 2 of the final office action, the Examiner indicated that a broad interpretation of "first data and second data" was taken to correspond to a first and second block of turbo code. The Examiner continues on page 3 to indicate that while only one block was shown in the flowcharts in figure 1 and 2 for simplicity, the exemplary block may be multiple turbo code blocks for iterations as shown in tables 1 and 2. Accordingly, SHIN's teaching is directed to the decoding of one or more blocks associated with the generation of a single response (ACK/NAK). However, SHIN does not explicitly disclose whether the plurality of blocks for a given H-ARQ process are decoded simultaneously by plural decoders or consecutively by a single decoder. For example, in paragraph 20, SHIN indicates that that when there are multiple Turbo code blocks in a H-ARQ process, a NACK for the H-ARQ process will be generated, if any one of code blocks is determined to diverge and then all the iterations with the rest of the blocks will be terminated as well. From the above language it is not clear whether the plurality of blocks for a given H-ARQ process are decoded simultaneously by plural decoders or consecutively by a single decoder. Nevertheless, regardless whether the plurality of blocks for a given H-ARQ process are decoded simultaneously by plural decoders or

consecutively by a single decoder, SHIN does not teach "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data **at a decoding start time of the second data**".

In consideration of interpreting SHIN as suggesting that a plurality of blocks for a given H-ARQ process are decoded simultaneously by plural decoders, SHIN inherently fails to teach "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data **at a decoding start time of the second data**". However, in consideration of interpreting SHIN as suggesting that a plurality of blocks for a given H-ARQ process are decoded consecutively by a single decoder, nothing is SHIN discloses that if the decoder is still in operation to decode the first data **at a decoding start time of the second data**, the decoding of the first data is interrupted at a predetermined time before a response (ACK/NAK) time delay of the first data expires. Therefore SHIN cannot read on the claim language of "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data".

Moreover, even if the Examiner could somehow interpret respective blocks of a separate H-ARQ processes as the first and second data, nothing in SHIN teaches "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data".

Furthermore, SHIN does not disclose interrupting the decoding of the first data at a predetermined time before **a response (ACK/NAK) time delay of the first data expires**. Specifically, SHIN does not disclose an expiration of a response (ACK/NAK) time delay. Instead, SHIN teaches that a response (ACK/NAK) occurs after a maximum number of iterations or may occur earlier if a lesser number of iterations converge. Applicants have reviewed the entirety of SHIN's disclosure and find nothing in SHIN that teaches an expiration of a response (ACK/NAK) time delay, let alone interrupting the decoding of the first data at a predetermined time before **a response (ACK/NAK) time delay of the first data expires.**

Therefore, based upon the above arguments, it is clear that SHIN does not anticipate "interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data" as recited in Applicants' claim 1. **Should the Examiner maintain the rejection, the examiner is respectfully requested to address each of the above arguments.** Further, should the Examiner maintain the rejection, the Examiner is respectfully requested to articulate in detail how SHIN is being interpreted as teaching each and every element of *"interrupting the decoding of the first data at a predetermined time before a response (ACK/NAK) time delay of the first data expires if the decoder is still in operation to decode the first data at a decoding start time of the second data"*.

In view of the above arguments, SHIN fails to anticipate each and every limitation of claim 1. Therefore, claim 1 is allowable over SHIN for the reasons given above and withdrawal of the rejection is hereby solicited. Independent claims 9, 21 and 22 comprise similar subject matter to that discussed above with respect to claim 1 and is therefore allowable for similar reasons. Dependent claims 2-8 and 10-16 are allowable for the reasons given above by virtue of their dependence on independent claims 1 and 12.

Furthermore, regarding claims, 18 and 20-22, these claims require: "a combined decoding time of the first and second data [that] is maximized". By contrast, in SHIN's teaching, the iterations of decoding for an H-ARQ process are minimized so as to generate the ACK/NACK response signal with minimal delay. Therefore, SHIN clearly does not teach that a combined decoding time of the first and second data is maximized. Should the Examiner reject the claims over SHIN the Examiner is respectfully requested to articulate in detail how SHIN is being interpreted as teaching each and every element of *"a combined decoding time of the first and second data [that] is maximized"*. Further, should the Examiner reject the claims 18 and 20-22 over SHIN and another prior art reference, the Examiner is respectfully requested to articulate in detail how SHIN does not teach away from the combination.

In view of the above arguments, SHIN fails to anticipate each and every limitation of claims 18 and 20-22. Therefore, claims 18 and 20-22 are allowable over SHIN for the reasons given above.

III. Conclusion

In view of the above, it is believed that the above-identified application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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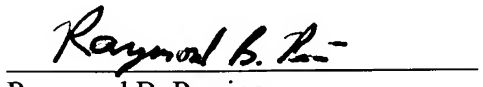

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